Complete RDS encoder in one chip

DESCRIPTION

The MRDS192 is a fully digital Radio Data System encoder based on a microcontroller driven by I^2C compatible bus. With a minimum of external parts it forms complete RDS encoder with wide range of special applications.

RDS SERVICES DIRECTLY SUPPORTED

- **PI** Program Identification
- **PS** Program Service
- **PTY** Program Type
- **TP** Traffic Program
- **AF** Alternative Frequencies
- **TA** Traffic Announcement
- **DI** Decoder Identification
- **M/S** Music/Speech
- **RT** Radiotext
- **User Defined Groups** (UDG, 2 modes)

CAPACITY

- AF: up to 15 items
- RT: 64 characters
- Dynamic PS text: up to 72 characters
- UDG: 2 groups (1 for each mode)
- Total capacity used by RDS data: 192 bytes

FEATURES

- Single supply
- Typical operating current: 9 mA @ 5 V
- Minimum external parts
- Industrial temperature range
- EEPROM memory for data storage during power-off
- External TA switch
- Indication LED output
- Both stereo and mono operation possible
- Digital 19 kHz pilot tone PLL with phase shift and lock bandwidth adjustment
- Parallel 8-bit D/A converter, 361 kHz sampling rate (over-sampled)
- Broadcast quality output signal
- Only simple output filter required
- RDS/RBDS signal: conforms to CENELEC EN50067
- Continuous RDS transmission during all operations
- Communication bus: I^2C compatible, internally software emulated, bi-directional operations
- bus speed: 0 - 600 Hz
- Buffered PS and UDG data
- 4 modes for dynamic/scrolling PS incl. word alignment and one-by-one character scrolling
- Packages available: 18-Pin PDIP, 18-Pin SOIC

APPLICATIONS

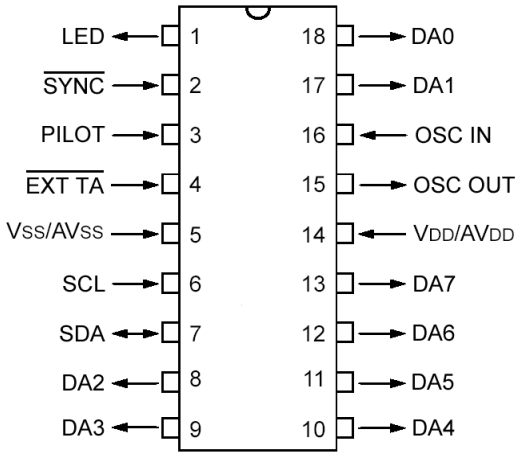
- Extremely low-cost FM broadcast RDS encoders
- Small all-in-one FM transmitters
- Private messaging systems
- RDS encoders for cable FM modulators
- Text output from any device to FM receiver
- Fixed RDS data encoding

Note: Consider following devices for new design: MRDS1322, PIRA32 Microcontroller

Revision 2010-12-30

1.0 PIN DIAGRAMS AND DESCRIPTION

18-Pin PDIP, 18-Pin SOIC



Pin Name	Description
DA0	D/A Converter bit 0
DA1	D/A Converter bit 1
DA2	D/A Converter bit 2
DA3	D/A Converter bit 3
DA4	D/A Converter bit 4
DA5	D/A Converter bit 5
DA6	D/A Converter bit 6
DA7	D/A Converter bit 7
EXT TA	External TA switch
LED	Indication LED
OSC IN	Crystal oscillator input
OSC OUT	Crystal oscillator output
PILOT	Pilot tone input
SCL	Serial Clock
SDA	Serial Data
SYNC	Pilot sync switch
V_{DD}/AV_{DD}	Positive supply
V_{SS}/AV_{SS}	Ground reference

2.0 ELECTRICAL CHARACTERISTICS

Maximum Ratings

Ambient temperature under bias ..... -55 °C to +125 °C
Storage temperature ..... -65 °C to +150 °C
Voltage on any pin with respect to V_{SS} (except V_{DD}, EXT TA, and PILOT) ..... -0.3 V to (V_{DD} + 0.3 V)
Voltage on V_{DD} with respect to V_{SS} ..... -0.3 V to +7.5 V
Voltage on EXT TA with respect to V_{SS} ..... 0 V to +13.25 V
Voltage on PILOT with respect to V_{SS} ..... 0 V to +8.5 V
Maximum current sourced by any output pin ..... 25 mA
Maximum current sunk by any output pin ..... 25 mA

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Supply voltage	4.2	-	5.5	V	
V_{IL}	Input Low Voltage	-	-	0.8	V	$4.5 \le V_{DD} \le 5.5$
	EXT TA, PILOT	V_{SS}	-	0.2 V_{DD}	V	
V_{IH}	Input High Voltage	2.0	-	V_{DD}	V	$4.5 \le V_{DD} \le 5.5$
	EXT TA, PILOT	0.8 V_{DD}	-	V_{DD}	V	
V_{OL}	Output Low Voltage	-	-	0.6	V	I_{OL} = 8.5 mA, V_{DD} = 4.5 V
V_{OH}	Output High Voltage	V_{DD} - 0.7	-	-	V	I_{OH} = -3.0 mA, V_{DD} = 4.5 V
E_D	EEPROM Endurance	-	1M	-	E/W	-40 °C to +85 °C
F_{OSC}	Oscillator Frequency	-	4.332	-	MHz	
F_S	D/A Converter sampling rate	-	361	-	kHz	
F_{CLK}	I^2C clock frequency	0	-	600	Hz	
T_{HIGH}/T_{LOW}	I^2C clock high/low time	800	-	-	µs	
T_{HD}/T_{SU}	I^2C hold/setup time	800	-	-	µs	
$T_{HD:DAT}$	I^2C data input hold time	0	-	-	µs	
T_{AA}	I^2C output valid from clock	-	-	800	µs	
T_{BUF}	I^2C bus free time	2	-	-	ms	
		180	-	-	ms	UDG2 group inserted
		620	-	-	ms	PS buffer written
		1000	-	-	ms	EEPROM store cmd.

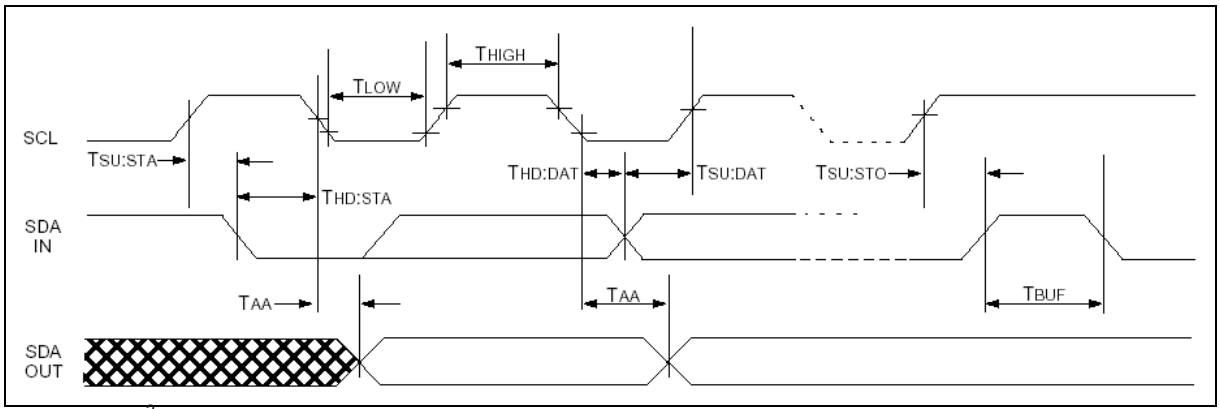


Figure 1.1 - I^2C bus timing

3.0 CONNECTION DIAGRAMS AND APPLICATION NOTES

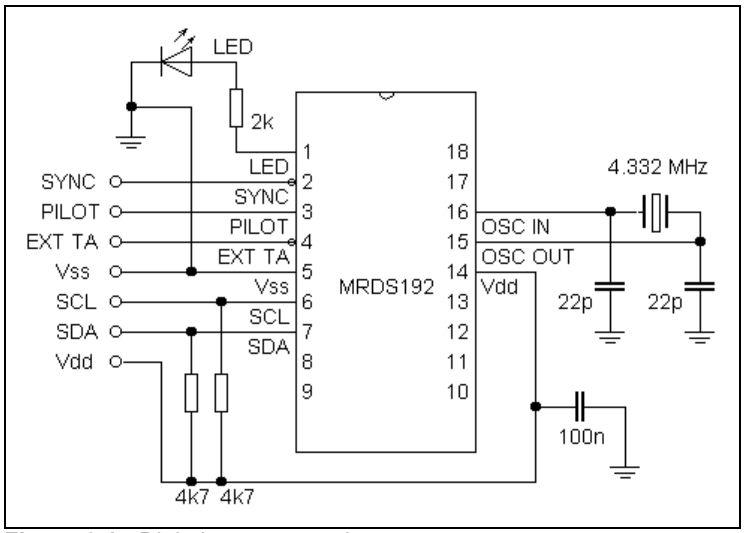


Figure 3.1 - Digital part connection

Operation LED

The LED indicates that the RDS encoder is in operation. It blinks approx. once per second.

It burns continuously during data transfers on I^2C bus.

Internal PLL

The MRDS192 includes an internal phase locked loop, which synchronises the RDS subcarrier with 19 kHz pilot tone in case of stereo transmission. Parameters of the PLL are controlled by software.

Pilot tone is tied to the PILOT input pin and must meet the levels specified by V_{IL} and V_{IH} parameters.

The PLL is active if the SYNC pin is driven low. This configuration makes easy to connect commonly available clock recovery circuits if the pilot tone needs to be filtered from MPX signal.

The PLL should be permanently disabled in case of mono transmission by connecting the SYNC pin to V_{DD} (directly or through a resistor).

External TA switch

The external TA switch can set the Traffic Announcement flag to 1. The TA flag is set to 1 if the EXT TA input is driven low. This can be done using simple mechanical switch (figure 3.2) or any logic circuit.

Where the external TA switch feature is not required, the EXT TA pin should be connected to V_{DD} (directly or through a resistor).

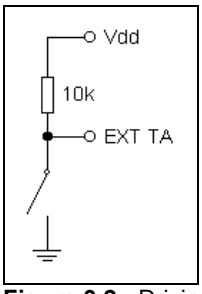


Figure 3.2 - Driving the TA flag by a mechanical switch

I^2C bus

The I^2C is a bi-directional bus used to transfer addresses and data into and out of the device. According to the bus specification the MRDS192 is a slave device driven by master (microcomputer, PC etc.). The master generates clock signal, START/STOP conditions, addresses and specifies if read or write operation will be performed.

All devices on I^2C bus are open drain terminals, therefore the bus requires pull-up resistors to V_{DD}.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START/STOP conditions.

Digital-to-Analog converter

The MRDS192 uses parallel 8-bit D/A converter with over-sampling technique. Digital data provided on DA pins can be directly formed into analogue output signal using low-cost resistor network.

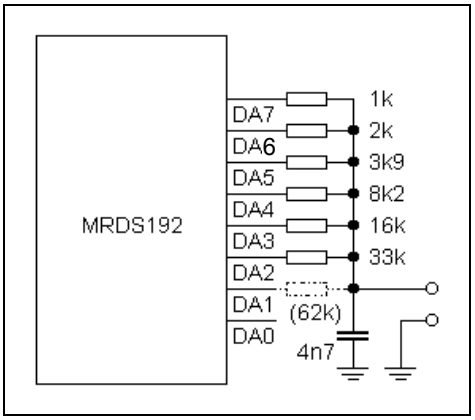


Figure 3.3 - 6 (or 7) bit D/A converter network

Figure 3.3 shows simple 6-bit D/A converter using six of binary weighted resistors. It contains one resistor for each bit of the DAC connected to a summing point. It's possible to add seventh resistor (62k) and form 7-bit DAC.

Figure 3.4 shows accurate 8-bit DAC using R/2R resistor network. It's a binary weighted DAC that creates each value with a repeating structure of 2 resistor values, R and R times two. This is an optimal DAC for this device.

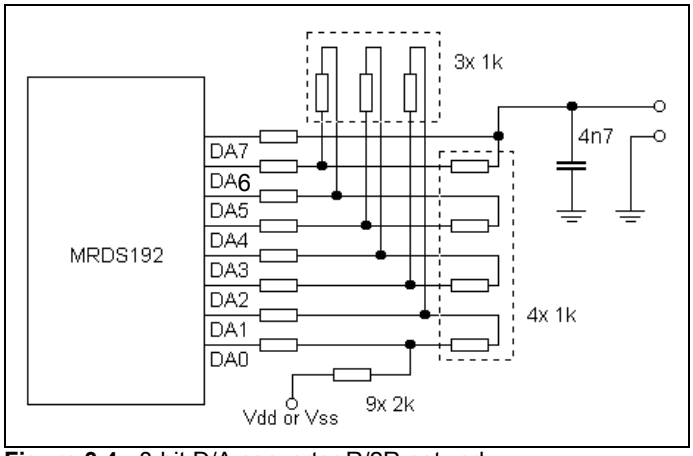


Figure 3.4 - 8-bit D/A converter R/2R network

Below is a table showing typical values accomplished with each DAC type. The values are measured in base-band on FM transmitter input. 0 dBc corresponds to the RDS signal main spectral component at 57 kHz. 0 dB corresponds to 75 kHz peak FM deviation; peak deviation caused by RDS: 3.4 kHz.

Parameter	6-bit	7-bit	8-bit R/2R
57 kHz output signal bandwidth	+/- 2.4 kHz (43 dBc)	+/- 2.4 kHz (45 dBc)	+/- 2.4 kHz (50 dBc)
Spurious suppression	> 74 dB	> 80 dB	> 90 dB

Note: Typical signal-to-noise ratio of FM broadcast transmitters is 70 – 80 dB.

Output low-pass filter

The output RDS signal modulated at 57 kHz subcarrier requires no special filtering. Spurious products are kept below -70 dB broadcast limit and the D/A conversion residues around the sampling frequency can be cut-off using any simple low-pass filter. This may be based either on active filter or a simple LC element. For FM broadcast purposes the low-pass filter rejection should be at least 20 dBc on the sampling frequency. It is recommended for high quality FM broadcasting that the output filter characteristics interpolate at least these values:

15 kHz	57 kHz	360 kHz
-20 dBc	0 dBc	**-30 dBc**

4.0 I²C CONTROL

Bus specification

The I²C bus implemented fully meets the I²C specification with respect to the bus timing specified in section 2.0. It's also compatible with I²C serial EEPROM's so the control algorithms can be the same.

Write operations

All write operations are performed in RAM so the number of write operations is unlimited. Storing the data to internal EEPROM memory is activated by a special command.
Number of bytes written in page write mode is limited only by access RAM boundaries. As a protective measure, internal address counter will not wrap around if the last byte accessible is reached.

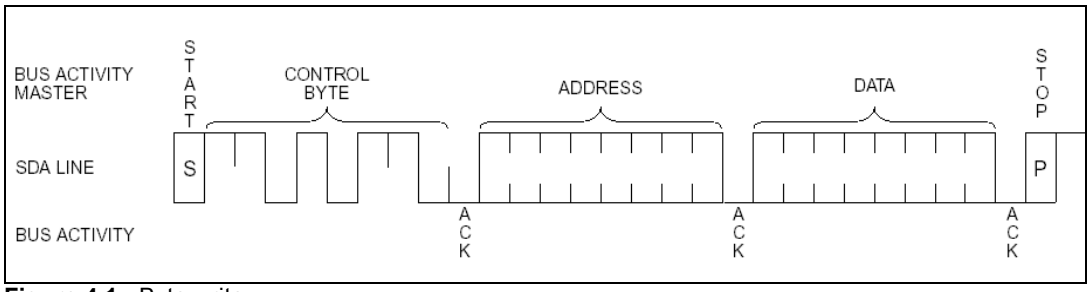


Figure 4.1 - Byte write

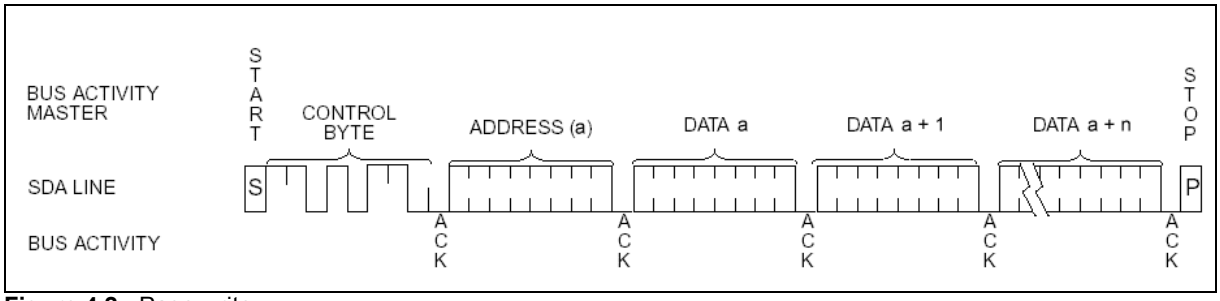


Figure 4.2 - Page write

Read operations

Read operations allow the master to access any RAM location. To perform the read operation, first the word address must be set. This is done by sending the word address to the MRDS192 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/W bit set to a one.

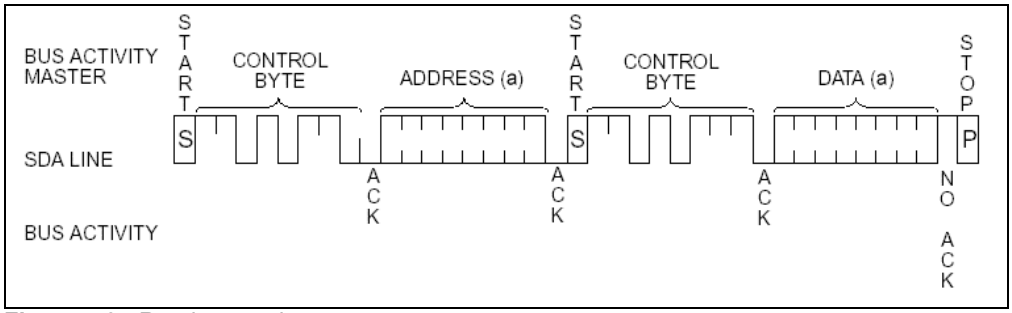


Figure 4.3 - Random read

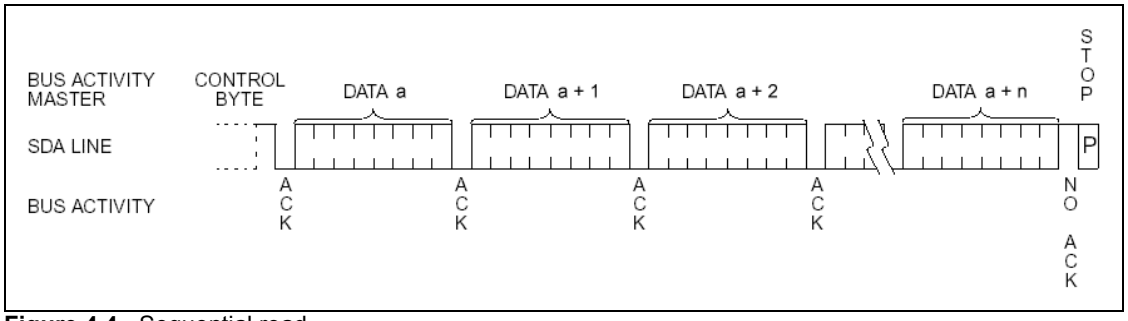


Figure 4.4 - Sequential read

Control byte

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 7-bit control code. For the MRDS192 this is set as 1101011 binary for read and write operations. The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

Operation	Control byte	
	Control code	R/W
Write	1101011	0
Read	1101011	1

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge (ACK) after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit. The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.
The MRDS192 does not generate any acknowledge bits during the device is busy (see the minimal values of T_{BUF} time in section 2.0). This can be used to determine when the device is ready and maximize the bus throughput.

More about I^2C:

[1] - The I^2C Bus Specification; Philips semiconductors, www.semiconductors.philips.com

[2] - 24LC04B/08B I^2C Serial EEPROMs datasheet; Microchip, www.microchip.com

5.0 COMMENTED MEMORY MAP

Address		Parameter	Description
HEX	DEC		
00-01	0-1	PI	Program Identification code. Identification code of the radio station. Always contains four hexadecimal digits.
02-09	2-9	PS Buffer	Program Service name (buffered). Static name of radio station that is displayed on receiver. Max. 8 characters long, redundant characters must be filled as spaces (32).
0A	10	PTY	Program Type (0-31). An identification number to be transmitted with each program item, intended to specify the current Program Type within 32 possibilities. Program type codes (Europe / US): 0 – (none) / (none) 1 – News / News 2 – Affairs / Information 3 – Info / Sports 4 – Sport / Talk 5 – Education / Rock 6 – Drama / Classic Rock 7 – Cultures / Adult Hits 8 – Science / Soft Rock 9 – Varied Speech / Top 40 10 – Pop Music / Country 11 – Rock Music / Oldies 12 – Easy Music / Soft 13 – Light Classics Music / Nostalgia 14 – Serious Classics / Jazz 15 – Other Music / Classical 16 – Weather / Rhythm and Blues 17 – Finance / Soft Rhythm and Blues 18 – Children / Foreign Language 19 – Social Affairs / Religious Music 20 – Religion / Religious Talk 21 – Phone In / Personality 22 – Travel / Public 23 – Leisure / College 24 – Jazz Music / (unassigned) 25 – Country Music / (unassigned) 26 – National Music / (unassigned) 27 – Oldies Music / (unassigned) 28 – Folk Music / (unassigned) 29 – Documentary / Weather 30 – Alarm Test / Emergency Test 31 – Alarm / Emergency
0B	11	DI	Decoder Identification (0-15).
0C	12	MS	Music/Speech switch (0/1). 0 - Speech program 1 - Music program
0D	13	TP	Traffic Program (0/1). This is a flag to indicate that the tuned program carries traffic announcements. The TP flag must only be set on programs that dynamically switch on the TA identification during traffic announcements. The signal shall be taken into account during automatic search tuning.
0E	14	TA	Traffic Announcement (0/1). Indicates instantaneous presence (1) of traffic information during broadcasting. When this value is set to 1 by external TA switch, the value specified by TA command has no effect. When this value is set to 1 by TA command, the value set by external TA switch has no effect.

0F	15	AFNUM	Number of Alternative Frequencies (0-15).
10-1E	16-30	AF	List of Alternative Frequency channels in hexadecimal range of 01-CC (87.6-107.9 MHz). Up to 15 items allowed.
1F	31	RTEN	Bit 0: Enables (1) or disables (0) the Radiotext. Bit 1: Controls the RT A/B type flag.
20-5F	32-95	RT	Radiotext. Up to 64 characters long text message to be displayed on receiver in Radiotext format. Redundant characters must be filled as spaces (32). Car radios usually don't support this service, Dynamic PS can be used instead.
60	96	UDG1EN	Enables (1) or disables (0) the UDG1 transmission.
61-66	97-102	UDG1 Buffer	User Defined Group 1 (buffered) Specifies one group in BBBBCCCCDDDD format, which is repeatedly transmitted by the RDS encoder. BBBB, CCCC and DDDD represent the contents of the block B, block C and block D. The RDS encoder calculates the CRC automatically. The block A has not been specified as it is always the PI code. The PTY and TP services set in the UDG2 group are ignored and are substituted according to the internal configuration of these services of the RDS encoder.
67-6C	103-108	UDG2 Buffer	User Defined Group 2 (buffered) Orders the RDS encoder to send directly RDS groups whose contents are free. The Group content is in BBBBCCCCDDDD format where BBBB, CCCC and DDDD represent the contents of the block B, block C and block D. The RDS encoder calculates the CRC automatically. The block A has not been specified as it is always the PI code. The PTY and TP services set in the UDG2 group are ignored and are substituted according to the internal configuration of these services of the RDS encoder. Using this command, the RDS transmission can then be partially controlled by an external application.
6D	109	UDG2START	When set to 1, the UDG2 group will be immediately inserted one time to the RDS stream from the buffer. Then this byte is automatically reset to 0. The buffer content will retain.
6E	110	EXTSYNC	External pilot synchronisation. Bit 0: 1 - Automatic external synchronisation if pilot tone present (default) 0 - Forced internal clock source (for mono transmission only) Bit 1: Controls the PLL lock range. 1 - 19000 +/- 2 Hz 0 - 19000 +/- 5 Hz - default
6F	111	PHASE	RDS Signal phase (0-18). Fixes the relative phase shift between the pilot tone and the RDS signal. Has effect only if bit 0 of the EXTSYNC is set to 1 and pilot tone is present. Changing the value by one results in 9.5 degrees phase shift change. The value serves only as a scale, it may not provide real phase shift value.
70	112	STATUS	Status register - read only. Bit 0: 1 - Pilot tone present 0 - Pilot tone not present or internal clock source set Bit 1: State of TA that is on air. Bit 2: Indicates if Dynamic PS text loop is running (1) or static PS is displayed (0).
71	113	CONTROL	Control register - write only. Depending on the value written the operation is performed. 69 (0x45, 'E'): Stores all RAM content to internal EEPROM. The content will be restored on next power-up. 82 (0x52, 'R'): Provokes a hardware reset of the RDS encoder and is equivalent to an "off-on" cycle of the RDS encoder. Must be the only byte written in the START-

			STOP session. 48 (0x30, '0'): Switches off the RDS subcarrier. Must be the only byte written in the START-STOP session. 49 (0x31, '1'): Switches on the RDS subcarrier.
72	114	SPSPER	Static PS period (0-255). Specifies the time between two repeats of the Dynamic PS text. Static PS (PS) is displayed during this time. Increasing the value by 1 increases the period by approx. 2.7 seconds. If value 255 is set, the Dynamic PS will be displayed only once, if the DPSNUM address is written.
73	115	DPSMOD	Display mode for the Dynamic PS text (0-3). 0 - Scrolling by fixed 8 characters 1 - Scrolling by 1 character 2 - Word alignment scrolling 3 - Scrolling by 1 character, text separated by spaces at begin and end *The dynamic PS text must be longer than 7 characters for mode **1**.*
74	116	LABPER	Label period in range of 0-255 used in Dynamic PS mode 0 and 2. Increasing the value by 1 increases the period by approx. 0.54 seconds.
75	117	SCRLSPD	Scrolling PS speed (0/1). Sets high (1) or low (0) speed of scrolling PS transmission (mode 1 and 3). Although setting high speed gives the result looking better, remember that on some receivers or under bad reception conditions the text may be unreadable. The reason is absolutely outside the RDS encoder and comes out from the fact that scrolling PS has never been included in RDS standard.
76	118	DPSNUM	Number of characters in Dynamic PS (0-72). When written, the Dynamic PS text loop is restarted.
77-BE	119-190	DPS	Dynamic PS. Up to 72 characters long text message to be displayed on receiver instead of static PS name. Can be used for song titles streaming etc. Before writing new text, set the DPSNUM to 0. After the text is written, set the DPSNUM to corresponding value.
C0-C7	192-199	PS	Program Service name (not buffered).

Notes:

- Buffered address range - Content of this address range is not directly used for the RDS transmission. If at least one byte from the address range is written, after STOP condition on the bus the content is copied to internal not buffered address range and synchronised with RDS groups order. This prevents transmission of partial content and mixing old and new values when the address range is written. The timing specified by T_{BUF} parameter must be considered (see section 2.0). For PS both buffered and not buffered address ranges are provided.

- Bit order:

MSB LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

6.0 SAMPLE APPLICATION CIRCUIT

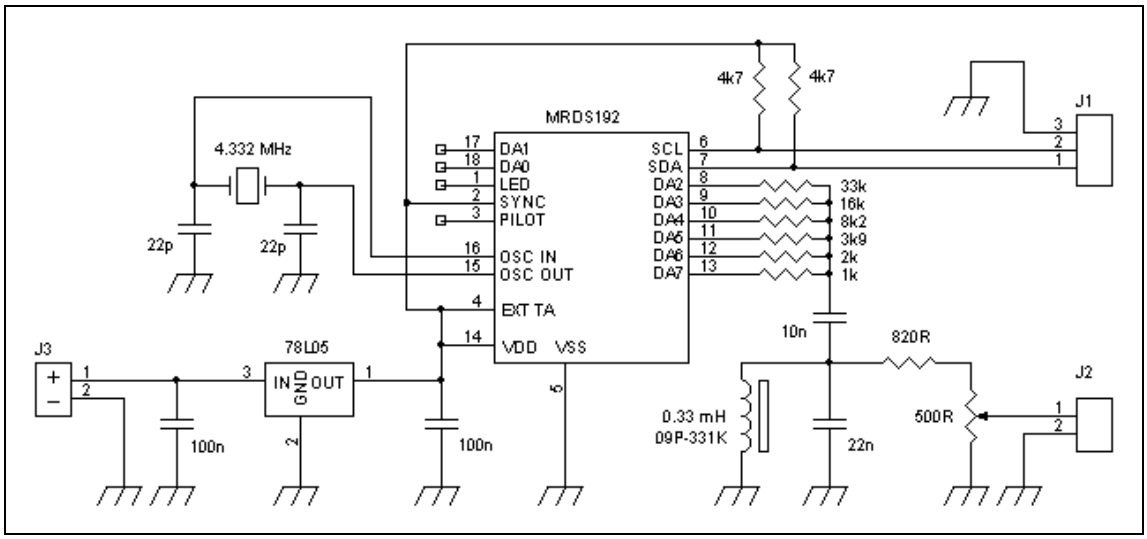


Figure 6.1 - Sample application circuit - schematic diagram

Notes:

- Power supply voltage (J3): 7-20 V
- Output RDS level (J2): 0-1.2 V p-p
- Output spectrum (6-bit DAC, FM deviation by RDS: 7 kHz):

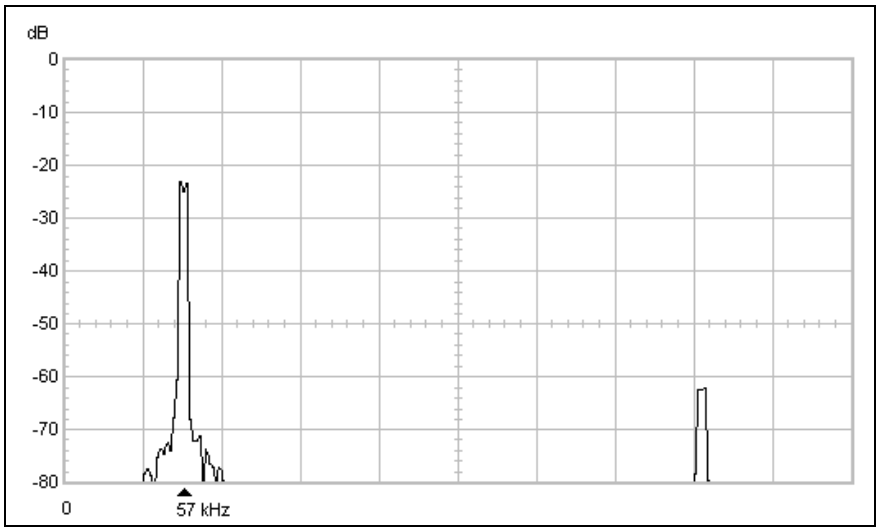


Figure 6.2 - Sample application circuit - output spectrum
(0 dB responds to 75 kHz deviation of FM carrier)